CLAIMS

Claims 1-20 (Cancelled)

21. (currently amended) An integrated circuit assembly for use in a system, wherein the integrated circuit assembly is configurable as a production part or as a development part, wherein the assembly comprises:

a first arrangement of connection terminals for connecting the integrated circuit to other components of the system;

debug circuitry; and

a debug interface comprising a second arrangement of connection terminals,

wherein for the development part configuration of the integrated circuit assembly, the second arrangement of connection terminals is adapted to be connected to a signal conversion arrangement for converting electrical signals provided to the second arrangement of terminals into a format for transmission to external monitoring circuitry using a communications link,

[and] wherein for the production part configuration of the integrated circuit assembly, the second arrangement of connection terminals is adapted such that no communications link is provided from the second arrangement of terminals to external monitoring circuitry, and wherein debug support resources of the integrated circuit assembly are accessed by the first arrangement of connection terminals,

and wherein the first and second arrangements of connection terminals together define a ring of terminals around the periphery of an upper surface of the assembly.

22. (currently amended) An assembly as claimed in claim 21 [[22]], wherein the signal conversion arrangement comprises electro-optical conversion means, and the communications link comprises an optical communications link.

23. (previously presented) An assembly as claimed in claim 22, wherein the electro-optical conversion means comprises an array of lasers.

24. (previously presented) An assembly as claimed in claim 23, wherein the lasers comprise vertical cavity surface emitting lasers.

25. (currently amended) An assembly as claimed in claim 21, wherein the integrated circuit assembly comprises, for both the development part configuration and the production part configuration, the signal conversion arrangement ~~means~~.

26. (previously presented) An assembly as claimed in claim 25, wherein the signal conversion means is integrated into a monolithic circuit of the integrated circuit assembly.

27. (previously presented) An assembly as claimed in claim 21, wherein the development part configuration is provided with the signal conversion arrangement and the production part configuration is not provided with the signal conversion arrangement.

28. (previously presented) An assembly as claimed in claim 21, wherein the signal conversion arrangement comprises analogue electrical circuitry for implementing digital communication over the communications link.

29. (previously presented) An assembly as claimed in claim 21, wherein the signal conversion arrangement comprises analogue electrical circuitry for providing a control signal for controlling an electro-optical conversion means.

30. (cancelled)

31. (currently amended) An assembly as claimed in claim 21 [[30]], wherein the second arrangement of terminals are formed from a top metal layer of the assembly.

32 [[22]]. (cancelled)

33. [[23]] (currently amended) An assembly as claimed in claim 21, further comprising a second integrated circuit memory device, comprising a third arrangement of

connection terminals connected to the first or second arrangement of connection terminals of the first integrated circuit, wherein the debug interface provides access to internal operation information of the first and second integrated circuits.

34. [[24]] (currently amended) A set of integrated circuits, comprising:

at least one first integrated circuit assembly as claimed in any preceding claim configured as a development part; and

a plurality of second integrated circuit assemblies as claimed in any preceding claim configured as production parts having the same design as the at least one first assembly in respect of the first arrangement of connection terminals and the debug interface, and wherein the plurality of second assemblies are not provided with the communications link of the at least one first assembly.

35. [[25]] (currently amended) A set as claimed in claim [[24]] 34, wherein the plurality of second integrated circuit assemblies have the same design as the at least one first assembly in respect of the debug circuitry.

36. [[26]] (currently amended) A method of performing a debug operation, using an integrated circuit assembly comprising a first arrangement of connection terminals, debug circuitry, and a debug interface comprising a second arrangement of connection terminals, the method comprising:

defining a ring of terminals around the periphery of an upper surface of the assembly, said ring of terminals being formed by the first and second arrangements of connection terminals;

coupling a signal conversion arrangement comprising electro-optical conversion means to the second arrangement of connection terminals;

using the signal conversion arrangement to convert electrical signals provided to the second arrangement of terminals into a second format which comprises an optical transmission format;

transmitting the signals using the second format to external monitoring circuitry; and

performing a debug operation using the external monitoring circuitry.

37. [[27]] (currently amended) A method as claimed in claim [[26]] 36, wherein the electro-optical conversion means comprises an array of lasers.

38. [[28]] (currently amended) A method as claimed in claim [[27]] 37, wherein the lasers comprise vertical cavity surface emitting lasers.